AMENDMENTS TO THE CLAIMS

Claims pending

- At time of the Action: Claims 1-10
- After this Response: Claims 1-10

Canceled or Withdrawn claims: None

Amended claims: None

New claims: None

1. **(Previously presented)** A circuit comprising a line driver having output terminals

connected to a load for supplying a transmit signal to the load and a line receiver having input terminals connected to the load for simultaneously receiving a receive signal from the load, an arrangement for canceling the transmit signal on the input terminals of the line receiver, the output terminals of the line driver being connected to the load via equal first impedances, the input terminals of the line receiver being connected to the load via equal first resistors and to respective ones of the line driver output terminals via equal second resistors, wherein

the first impedances are complex impedances of an impedance value that is much smaller than an impedance value of the load so that a drive/termination impedance of the line driver matches the load impedance, and

transconductance amplifiers are provided to sense the voltage across the first impedances and supply corresponding currents to respective ones of the line driver input terminals.

2. **(Previously presented)** The circuit according to claim 1, wherein the drive/termination impedance of the line driver equals the impedance value of one of the first impedances multiplied by k, wherein k is a function of the line driver gain and the transconductance amplifier gains.

3. **(Previously presented)** An echo canceling arrangement comprising:

a line driver having two inputs and two outputs,

a load coupled with the outputs of the line driver via first and second impedances,

a line receiver having two inputs, wherein the inputs are coupled through a network with the load and the outputs of said line driver,

first and second transconductance amplifiers having two inputs and an output, wherein the inputs of the first transconductance amplifier are coupled with the first impedance and its output with the one input of the line driver and the inputs of the second transconductance amplifier are coupled with the second impedance and its output with the other input of the line driver,

wherein the first and second impedances are complex impedances of an impedance value that is much smaller than an impedance value of the load so that a drive/termination impedance of the line driver matches the load impedance.

4. **(Original)** The echo canceling arrangement according to claim 3, wherein the network comprises:

a first resistor coupled between one input of the line receiver and the load,

a second resistor coupled between the one input and one output of the line driver,

a third resistor coupled between the other input of the line receiver and the load, and

a fourth resistor coupled between the other input and the other output of the line driver.

5. **(Previously presented)** The echo canceling arrangement according to claim 3, wherein the first and third resistors are equal and the second and fourth resistors are equal.

6. **(Previously presented)** The echo canceling arrangement according to claim 3, wherein the drive/termination impedance of the line driver equals the impedance value of one of the first or second impedances multiplied by k, wherein k is a function of the line driver gain and the transconductance amplifier gains.

7. **(Previously presented)** An asymmetric digital subscriber line (ADSL) driver receiver circuit comprising:

an ADSL driver having two inputs and two outputs,

a load coupled with the outputs of the driver via first and second impedances,

an ADSL receiver having two inputs, wherein the inputs are coupled through a network with the load and the outputs of said driver,

first and second transconductance amplifiers having two inputs and an output, wherein the inputs of the first transconductance amplifier are coupled with the first impedance and its output with the one input of the driver and the inputs of the second transconductance amplifier are coupled with the second impedance and its output with the other input of the driver,

wherein the first and second impedances are complex impedances of an impedance value that is much smaller than an impedance value of the load so that a drive/termination impedance of the line driver matches the load impedance.

8. **(Original)** The circuit according to claim 7, wherein the network comprises:

a first resistor coupled between one input of the receiver and the load,

a second resistor coupled between the one input and one output of the driver,

a third resistor coupled between the other input of the receiver and the load, and

a fourth resistor coupled between the other input and the other output of the driver.

9. **(Previously presented)** The circuit according to claim 7, wherein the first and third resistors are equal and the second and fourth resistors are equal.

10. **(Previously presented)** The circuit according to claim 7, wherein the drive/termination impedance of the driver equals the impedance value of one of the first or second impedances multiplied by k, wherein k is a function of the driver gain and the transconductance amplifier gains.